MITSUBISHI

PROGRAMMABLE CONTROLLER

MELSEC-K

Instruction Manual

RS-232C Computer Link Unit type KJ71L7

(NA) 66015-A

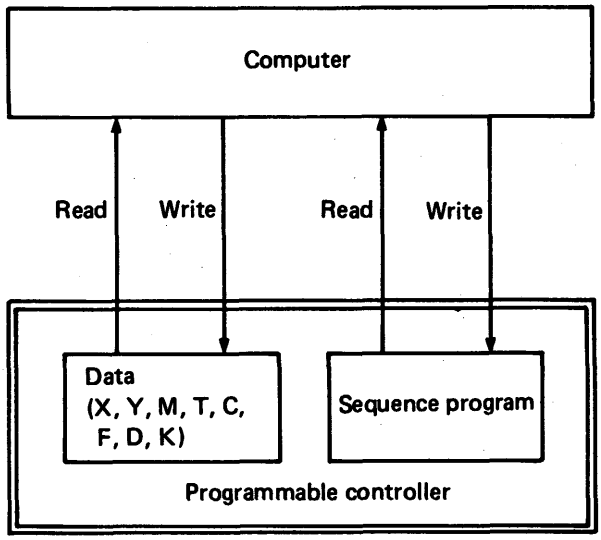
MITSUBISHI ELECTRIC

CONTENTS

1. GENERAL DESCRIPTION

1. GENERAL DESCRIPTION

This instruction manual explains the specifications and operating procedures of Type KJ71L7 computer link unit (hereinafter referred to as KJ71L7) which is utilized to send and receive signals between a programmable controller (K3(N)CPU, K2NCPU, K2HCPU, or K2CPU-S3) and a computer such as a personal computer.
The KJ71L7 is designed to monitor the operating conditions of a programmable controller on the computer side and also to read and rewrite the contents of data registers and other devices. The KJ71L7 is capable of reading X, Y, M, T, C, D, F, and K and writing Y, M, T, C, D, F, and K. The KJ71L7 is also capable of reading and writing a sequence program.
Please prepare the program of computer for the transmission control protocol of programmable controller on user side.



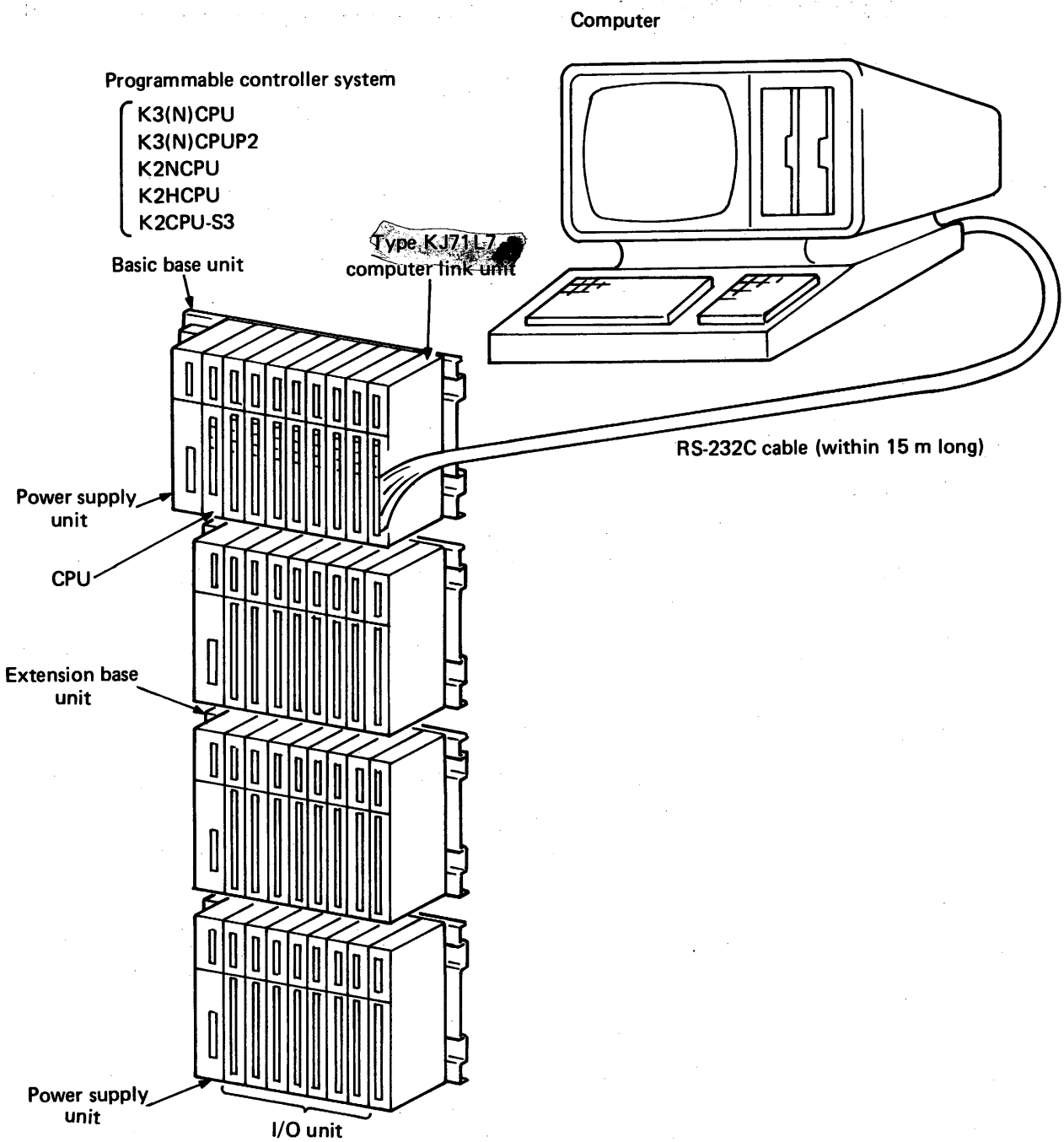
Compatible with the conventional Type KJ71L4 computer link unit, the KJ71L7 can be readily used instead of the KJ71L4.

The KJ71L7 has been changed in the following points:

(1) Four types of protocols are available.
(2) Sum check can be made as an error check function.
(3) Transmission sequence has been changed.
(4) The contents of LED displays have been changed.

2. SYSTEM CONFIGURATION

2. SYSTEM CONFIGURATION



WARNING

1. The KJ71L7 can be loaded into any desired slot of basic base unit except the slot "0".
2. The KJ71L7 can also be loaded into any desired slot of extension base unit.
3. The KJ71L7 cannot be loaded into the base unit of remote I/O system.
4. Only one unit of KJ71L7 can be loaded into one programmable controller system.
5. The KJ71L7 cannot be used with the KD51 in the same channel.
6. When the KJ71L7 is used for the K2N system, set the processing time setting pin of K2NCPU to the "SLOW" position.

3. SPECIFICATIONS

3. SPECIFICATIONS

3.1 General Specifications

Item	Specifications
Operating ambient temperature	0 to 55°C
Storage ambient temperature	–10 to 75°C
Operating ambient humidity	10 to 90%RH (no dew condensation)
Storage ambient humidity	10 to 90%RH (no dew condensation)
Vibration resistance	Conforms to class 3, IIB, JIS C 0911 (16.7 Hz, 3-mm double amplitude, 2 hrs.)
Shock resistance	Conforms to JIS C 0912 (10 g x 3 times in X, Y, and Z directions)
Noise resistance	1000 V_{P-P} noise voltage, 1 μs noise width, 25 to 60 Hz noise frequency by noise simulator
Operating ambience	To be free from corrosive gases. Dust should be minimal.
External connection method	20-point terminal block connector (M3 x 6 screw)
5V DC current consumption	0.8 A
Number of exclusively used points	32
Weight	0.62 kg

Table 3.1 General Specifications

CAUTION

The exclusively used I/O points of KJ71L7 are 32. By loading the KJ71L7, 32 I/O points of the corresponding slot are exclusively used.

3.2 Transmission Specifications

Item		Specifications	
Interface		Conforms to EIA RS-232C.	
Transmission method		Semi-double transmission system, specifically used protocol (character mode)	
Synchronous method		Asynchronous mode	
Transmission speed		1200, 2400, 4800, 9600 BPS (bits per second) selectable by switch	
Trans-mission symbols	Start bit	1	
	Data bit	7 (ASCII code)	
	Parity bit	1 or no parity bit	Either bit selected
	Stop bit	1 or 2	
Access cycle		90 ms/10 bytes on average (with respect to programmable controller—for details, see Section 5.6.)	
Accessed contents	Read	X, Y, M, T, C, D, F, K(*) and sequence program	
	Write	Y, M, T, C, D, F, K and sequence program	
Error detection		Parity check or no parity check (odd parity)	
		Sum check or no sum check	
Transmission distance		Within 15 m	

Note(*): X stands for input, Y for output, M for temporary memory, T for timer, C for counter, F for external failure memory, D for data register, and K for master control.

Table 3.2 Transmission Specifications

MEMO

4. HANDLING

4. HANDLING

4.1 Nomenclature of KJ71L7 Components

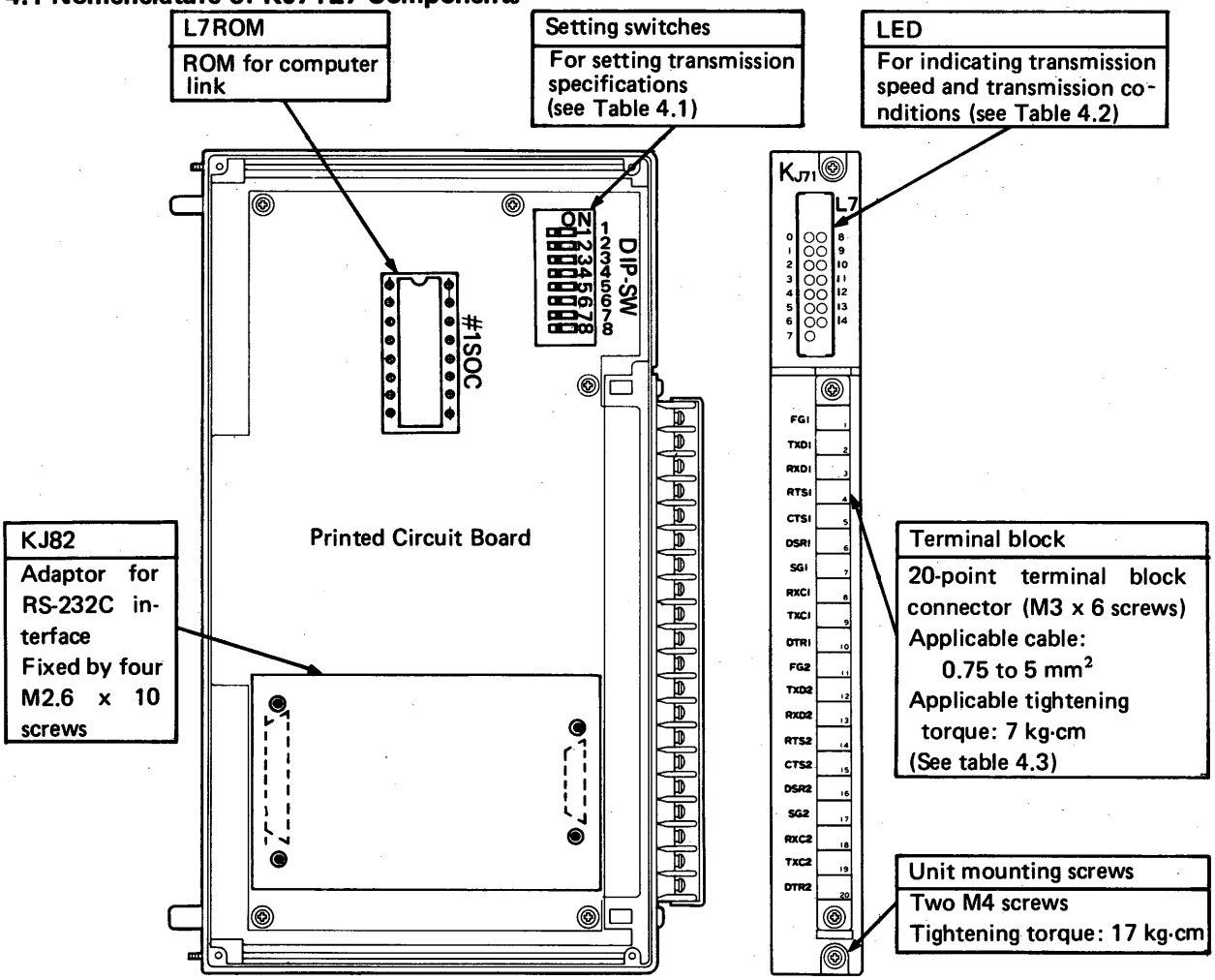


Fig. 4.1 KJ71L7

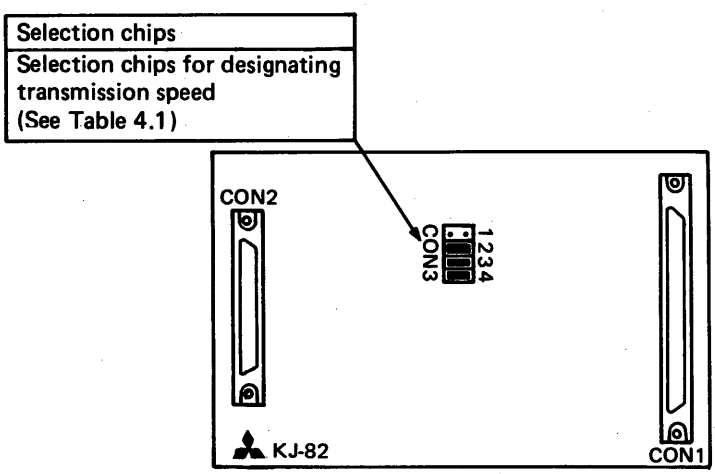
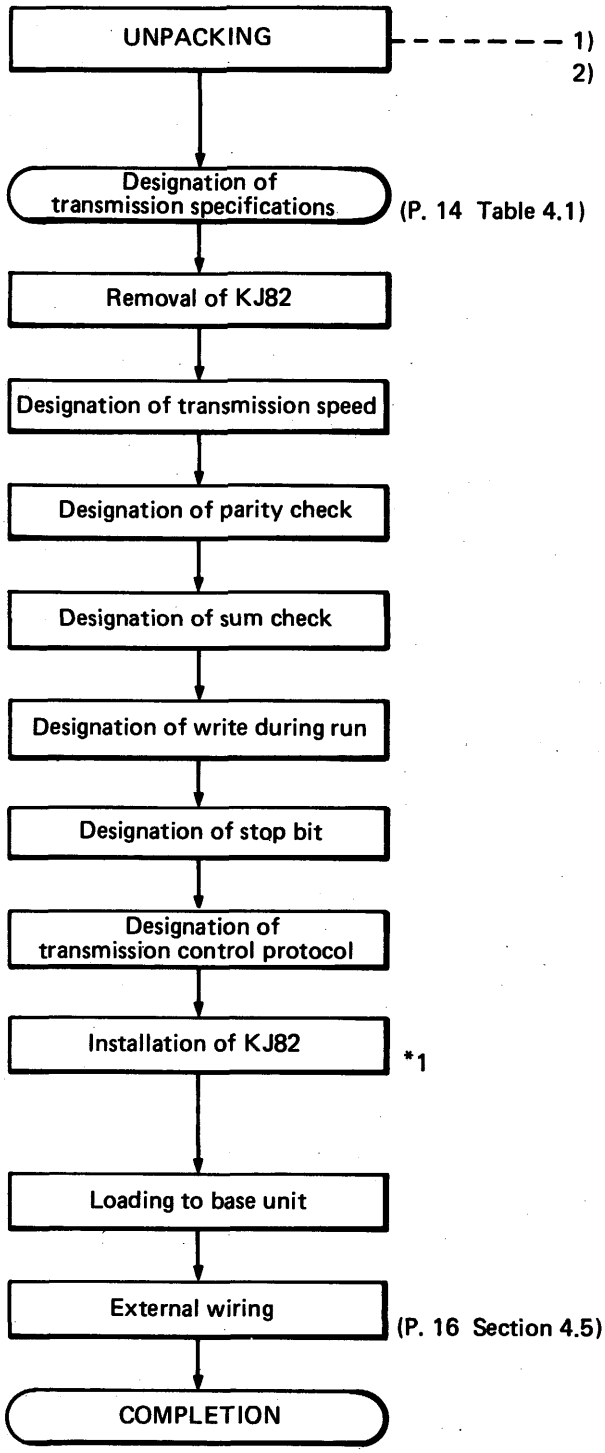


Fig. 4.2 KJ82

NOTE

1. All setting switches "DIP-SW" are factory-set to OFF position.
2. The selection chips of KJ82 are factory-set to 2, 3, and 4 positions.
3. When changing transmission speed, be sure to remove the KJ82.

4.2 Loading Procedure



CAUTION

*1: Load the KJ82 to the lower connectors. Load the KJ82 with care because the right and left connectors are different in size. (P.12. Fig. 4.1)

4.3 Designation of Transmission Specifications

		Setting Switch (DIP-SW)		Selection Chip of KJ82 (CON3)			
		Number	State	1	2	3	4
Transmission speed (bps)	1200	1	OFF	●		●	●
	2400				●	●	●
	4800		ON	●		●	●
	9600				●	●	●
Parity check	Not made	2	OFF				
	Made		ON				
Sum check	Not made	3	OFF				
	Made		ON				
Write during run of programmable controller	Possible	4	OFF				
	Impossible		ON				
Stop bit	1 bit	5	OFF				
	2 bits		ON				
(Empty)		6	OFF				
Transmission control protocol (See Section 5.1)		7	8				
	Type 1	OFF	OFF				
	Type 2	ON	OFF				
	Type 3	OFF	ON				
	Type 4	ON	ON				

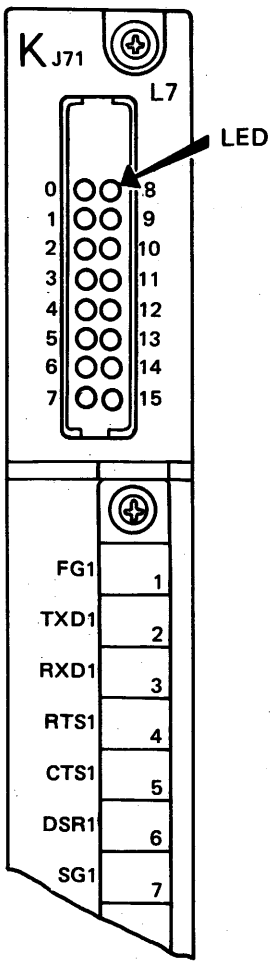
(● mark shows setting position of selection chip.)

Table 4.1 Designation of Transmission Specifications

CAUTION

1. Designate transmission speed by use of both setting switch (DIP-SW) and selection chips (CON 3) inside KJ82.
2. To designate transmission speed on the computer side, turn off the selection chips "3" (receiving clock) and "4" (sending clock) inside KJ82 (remove the chips).
3. Be sure to keep the switch "6" of KJ71 at OFF position.
4. Designate the type of transmission protocol by use of the switches "7" and "8" on KJ71. For details of protocol type, see Section 5.1.

4.4 LED Signal Names and Display Contents



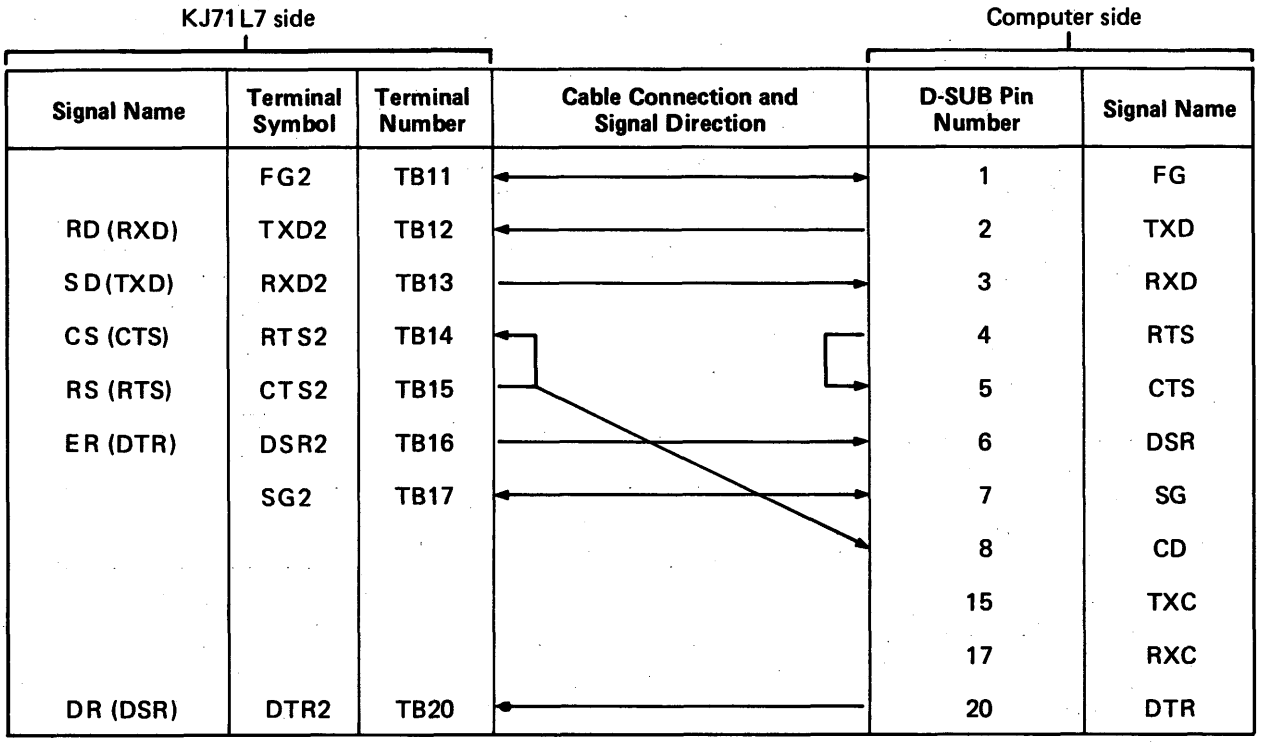
LED No.	Signal Name	Content
0	Sending	Lit during sending of data to computer.
1	Receiving	Lit during receiving of data from computer.
2	Communicating	Lit during communication with programmable controller CPU.
3	Neutral	Lit when transmission sequence is in initial state.
4	SW1	Display the states of transmission specification setting switches (DIP-SW) 1 to 4. Lit when switch is moved to ON position.
5	SW2	
6	SW3	
7	SW4	
8	ACK	Lit when "ACK" is sent to computer and turned off when "NAK" is sent.
9	NAK	Lit when "NAK" is sent to computer and turned off when "ACK" is sent.
10	Circuit error	Lit when communication error is detected and turned off when communication is normal.
11	(Empty)	
12	SW5	Display the states of transmission specification setting switches (DIP-SW) 5, 6, and 8. Lit when switch is moved to ON position.
13	SW6	
14	SW8	
15	(Empty)	

Table 4.2 LED Display Contents of KJ71L7

4.5 Connection of KJ71L7 with Computer

(1) The hardware specifications of KJ71L7 conform to EIA RS-232C.

(2) Connect the KJ71L7 and the computer according to Table 4.3.



KJ71L7 side				Computer side	
Signal Name	Terminal Symbol	Terminal Number	Cable Connection and Signal Direction	D-SUB Pin Number	Signal Name
	FG2	TB11	←	1	FG
RD (RXD)	TXD2	TB12	←	2	TXD
SD (TXD)	RXD2	TB13	→	3	RXD
CS (CTS)	RTS2	TB14	←	4	RTS
RS (RTS)	CTS2	TB15	→	5	CTS
ER (DTR)	DSR2	TB16	→	6	DSR
	SG2	TB17	←	7	SG
				8	CD
				15	TXC
				17	RXC
DR (DSR)	DTR2	TB20	←	20	DTR

Table 4.3

Note 1: The terminal symbols of KJ71L7 are matched to the signal names of the computer. Within the KJ71L7, therefore, the signal names of KJ71L7 are as shown in Table 4.3.

Note 2: The terminal numbers of KJ71L7, TB1 to TB10, TB18, and TB19, are not used.

Note 3: Connect the shielding of connection cable to the terminal TB11 (FG2) of KJ71L7.

Note 4: Output from KJ71L7
(1) RTS (request to send - TB15) turns on when the hardware of KJ71L7 is ready.

(2) DTR (data terminal ready - TB16) turns on when the KJ71L7 is ready for receiving data.

Note 5: Input to KJ71L7 (procedure by DSR (data set ready))

When DSR (TB20) turns off, transmission sequence is initialized. Normally, therefore, always keep DTR of the computer on. +3 to +15 V are "on" states and –3 to –15 V are "off".

Note 6: Signal name abbreviations

SD (TXD):	*Send data*
RD (RXD):	*Receive data*
RS (RTS):	*Request to send*
CS (CTS):	*Clear to send*
CD:	*Carrier detect*
ER (DTR):	*Data terminal ready*
DR (DSR):	*Data set ready*
SG:	*Signal ground*
FG:	*Frame ground*

MEMO

5. LINK METHOD OF KJ71L7 WITH COMPUTER

5. LINK METHOD OF KJ71L7 WITH COMPUTER

5.1 Transmission Control Protocol

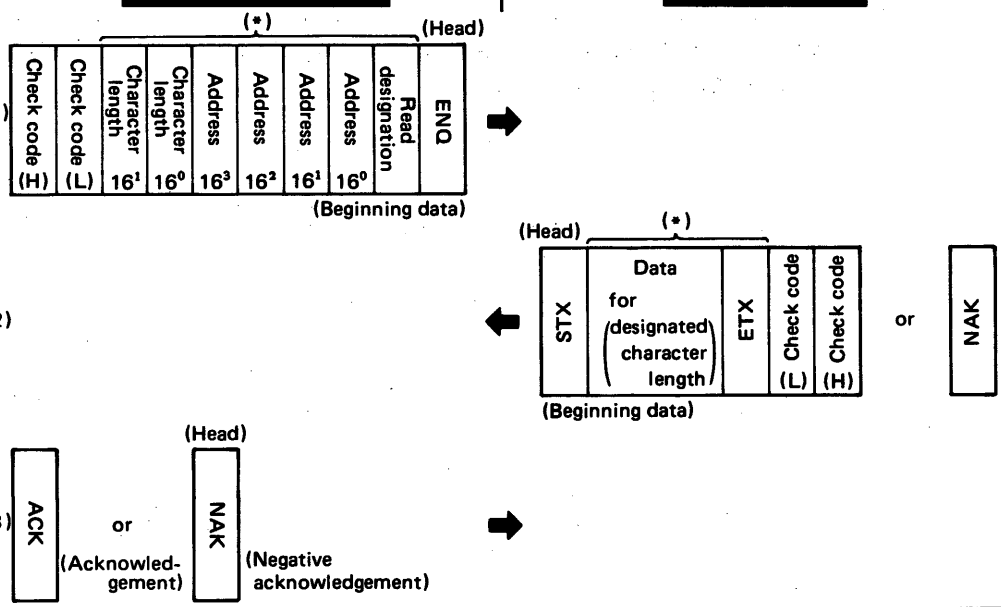
Transmission must always be triggered by the computer. Transmission cannot be triggered by the KJ71L7. By selecting the positions of setting switches (DIP-SW) 7 and 8, one of the following four protocol types can be selected.

(1): Type 1

Switch 7	OFF
Switch 8	OFF

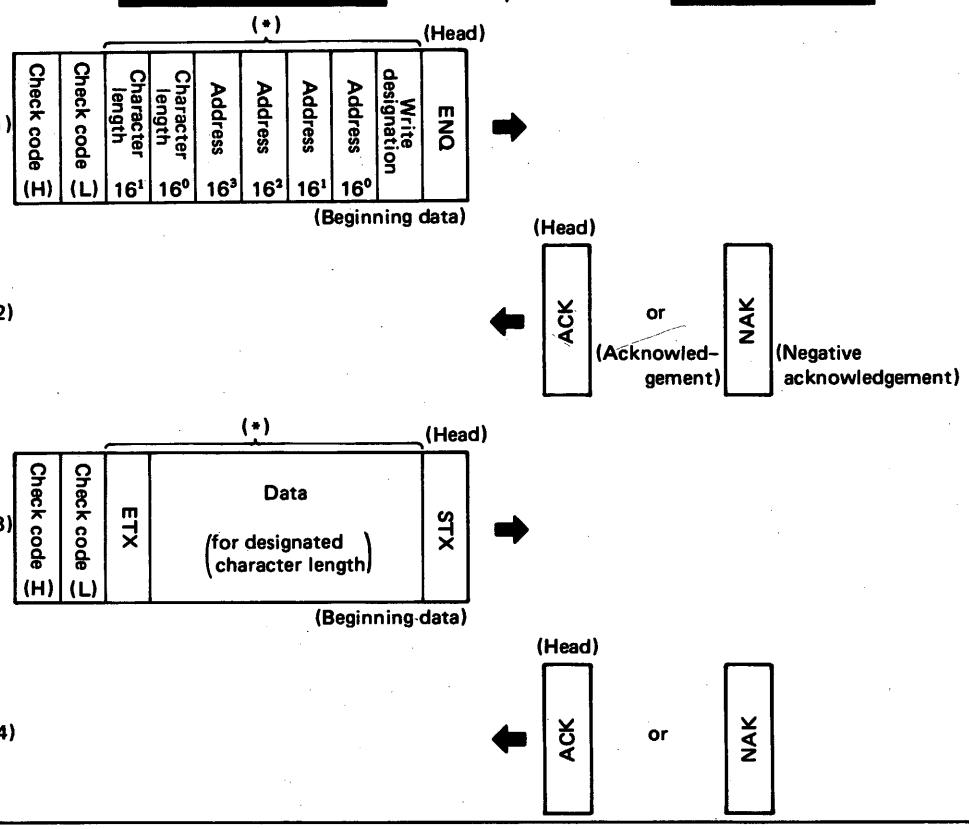
READ

1) Protocol for reading data of programmable controller by computer



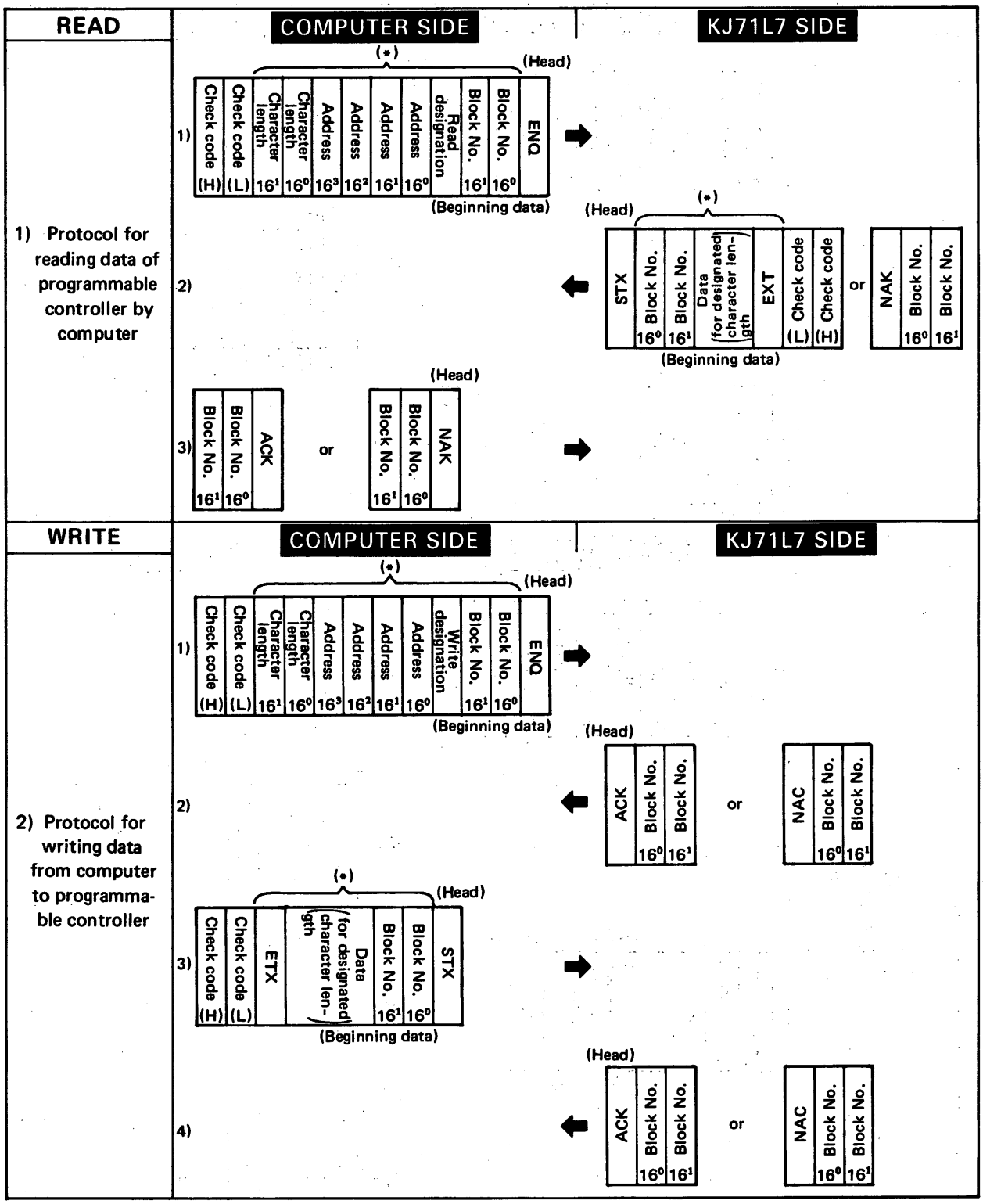
WRITE

2) Protocol for writing data from computer to programmable controller



(2) Type 2

Switch 7	ON
Switch 8	OFF

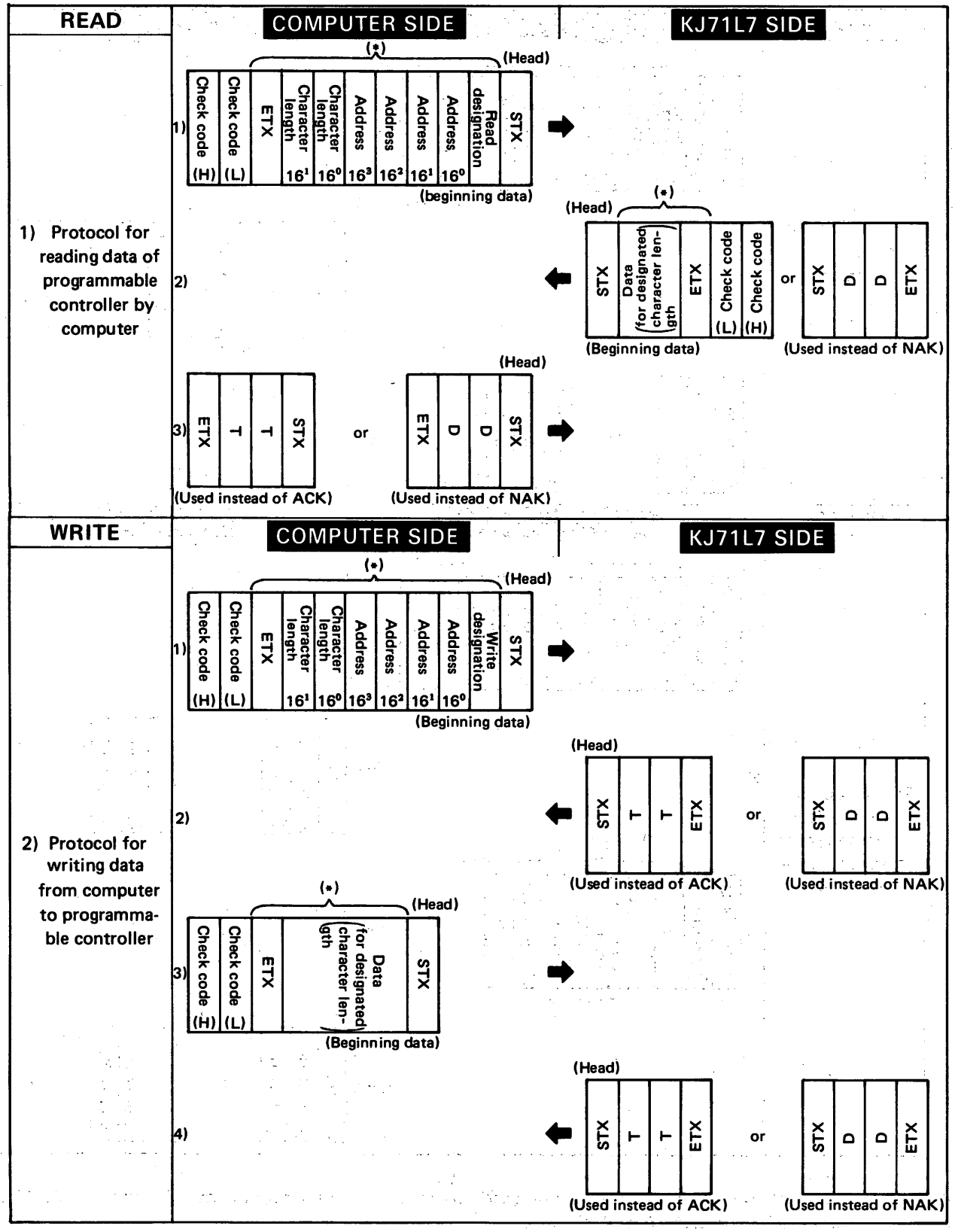


Note 1) The block number is an optionally assigned number for corresponding access. Also transmit the block number after converting it to ASCII code.

Note 2) Check code is provided only when sum check is specified.

(3) Type 3

Switch 7	OFF
Switch 8	ON

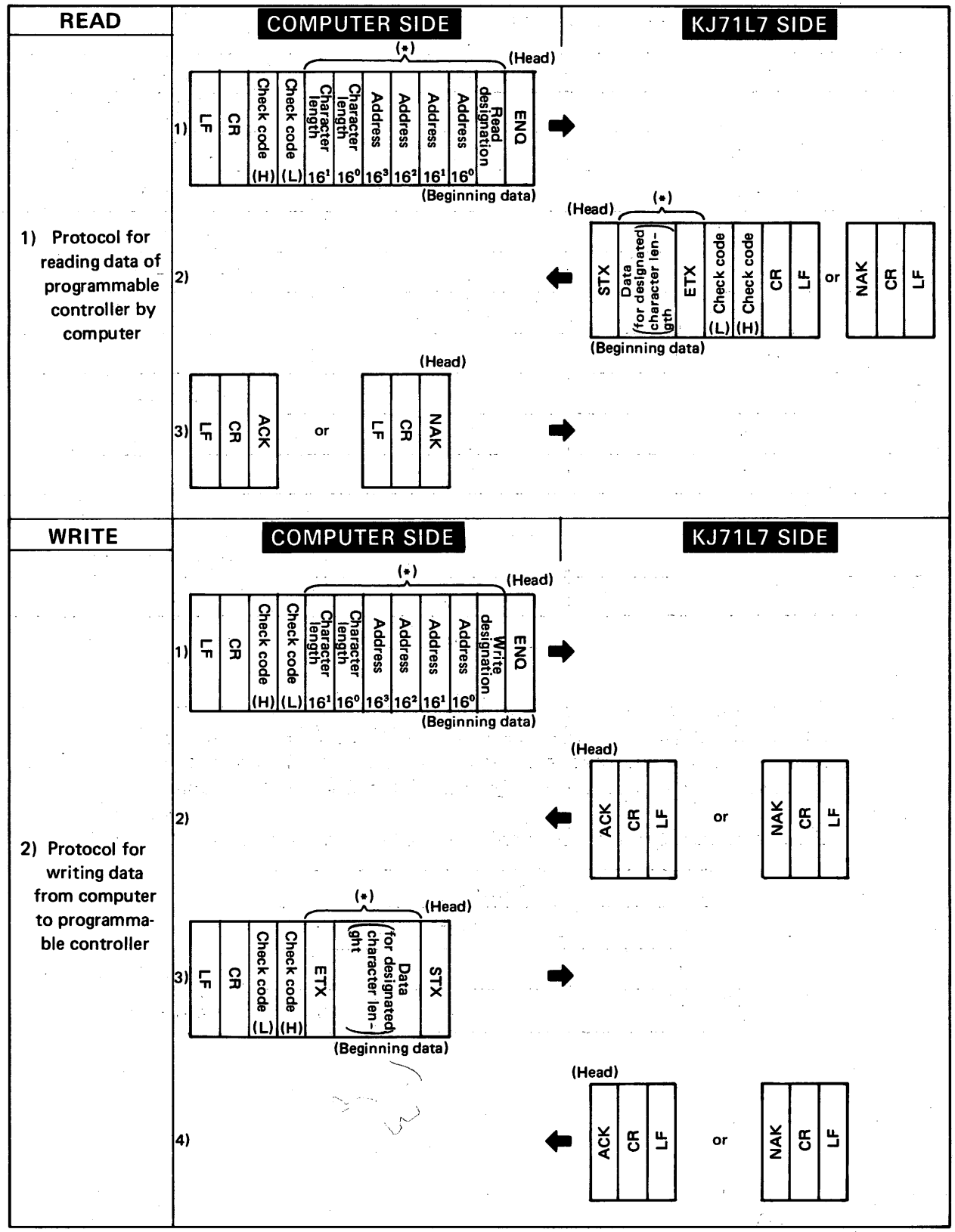


Note 1) Type 3 uses "T.T" instead of "ACK" and "D.D" instead of "NAK". Make up each data so that "STX" is located at the beginning and "ETX" at the end.

Note 2) Check code is provided only when sum check is specified.

(4) Type 4

Switch 7	ON
Switch 8	ON



Note 1) Type 3 uses "T.T" instead of "ACK" and "D.D" instead of "NAK". Make up each data so that "STK" is located at the beginning and "ETX" at the end.

Note 2) Check code is provided only when sum check is specified.

*Note 1: The check code is sum check. Make sum check for the characters indicated by * mark. For the specifications of sum check, see Section 5.3.*

Note 2: Transmission codes are as follows:

Signal	Code	Remarks
ENQ	05 H	Enquiry
STX	02 H	Start of Text
ETX	03 H	End of Text
ACK	06 H	Acknowledge
NAK	15 H	Negative Acknowledge
Write designation	11 H	
Read designation	12 H	
CR	0D H	Carriage Return
LF	0A H	Line Feed
T	54 H	
D	44 H	
EOT	04 H	End of Transmission
CL	0C H	Clear

(Hstands for hexadecimal digit.)

Note 3: The address means a storage location (internal address) of read or written data in the programmable controller. For the internal addresses of each CPU, see Section 5.2. Each storage location addresses the beginning data. The internal address is indicated in hexadecimal 4 digits. Send each digit after converting it to ASCII code.

Example: Addressing when internal address of programmable controller is 71F0H

Address				
16^3	16^2	16^1	16^0	
7	1	F	0	⇦ Hexadecimal digit
37H	31H	46H	30H	⇦ ASCII code

5.2 Internal Addresses and Data Configuration of Programmable Controller

		K2NCPU, K2CPU-S3, K2HCPU		K3(N)CPU	
		Device Number	Memory Address	Device Number	Memory Address
Process input		X0 to 1FF	6800H to 69FFH	X0 to 7FF	4800H to 4FFFH
Process output	Write	Y0 to 1FF	6800H to 69 FFH	Y0 to 7FF	5000H to 57FFH
	Read		6400H to 65FFH		
Temporary memory		M0 to 255	7000H to 70FFH	M0 to 1023	5800H to 5BFFH
Temporary value of timer, counter		T.C0 to 127	7100H to 71FFH	T.C0 to 255	5D00H to 5EFFH
Contact, coil of timer, counter		T.C0 to 127	7400H to 747FH	T.C0 to 255	5C00H to 5CFFH
Data register		D0 to 95*	7200H to 72FFH	D0 to 999*	4000H to 47CFH
External failure memory		F0 to 99*	7300H to 7363H	F0 to 99*	5F00H to 5F63H
Master control		K0 to 63	7500H to 753FH	K0 to 63	5FC0H to 5FFFH
Sequence program		–	4000H to 5FFFH	–	8000H to F999H

Note 1: "H" of 6800H, for example, indicates that "6800" is a hexadecimal numeral.

CAUTION

*: In regards to D and F for special use, access from the computer is also possible. In this case, however, use them with care in accordance with application purpose.

Table 5.1 Internal Addresses of Programmable Controller

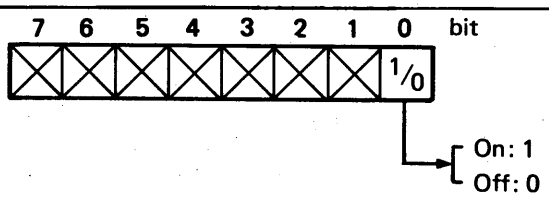
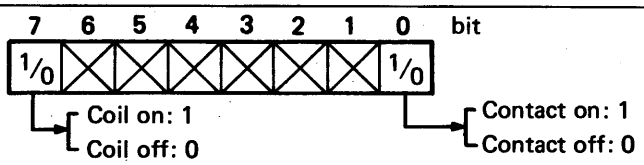
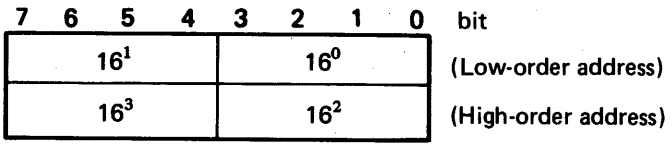
Device	Data Configuration
Process input/output (X/Y) Temporary memory (M) External failure memory (F) Master control (K)	
Contact, coil of timer counter (T, C)	
Temporary value of timer, counter (T, C) Data register	

Table 5.2 Data Configuration

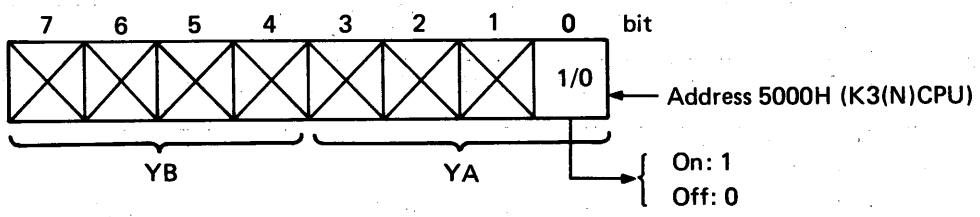
Note 2: The bit data indicated by (☒) marks in data configuration are ignored by the programmable controller. Therefore, also mask these data in the computer.

Example: Transfer of data in temporary memory M0

Computer side ← KJ71L7 side

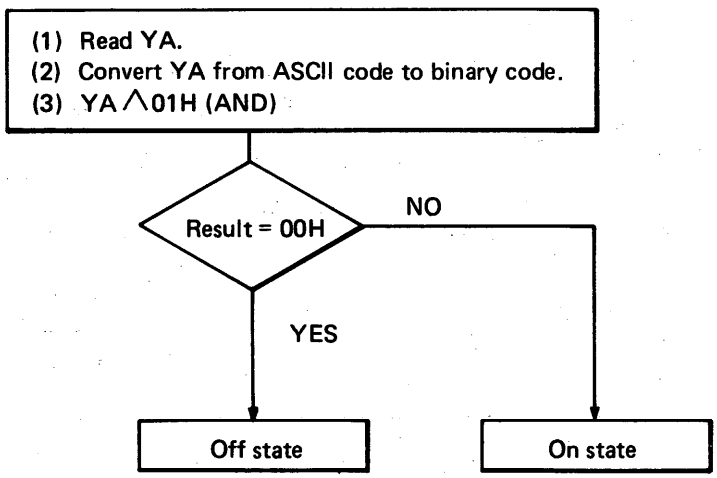
STX	Data (M0)		ETX	Check code (L)	Check code (H)
	16^0	16^1			
02H	YA	YB	03H	※	※

YA and YB are data converted into ASCII code.
※mark indicates the sum check code of data and ETX.



Internal State of Programmable Controller		Data Converted into ASCII Code		
		YB	YA	
Off state	00	30H	30H	Indicated by either of these codes
	FE	46H	45H	
On state	01	30H	31H	Indicated by either of these codes
	FF	46H	46H	

Therefore, to judge whether the interior of programmable controller is on or off,

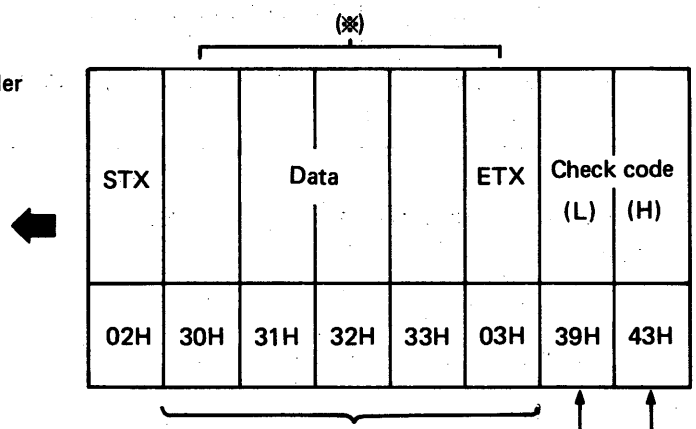


5.3 Specifications of Sum Check

The characters indicated by ※mark in Section 5.1 are added in terms of binary (pure binary) values and the low-order 1 bytes of the result are divided into 4 bits of [bit 0 to 3] and [bit 4 to 7]. These bits are converted into 2-byte ASCII codes, respectively and added as check codes to the address located after the character indicated by ※mark.

Example

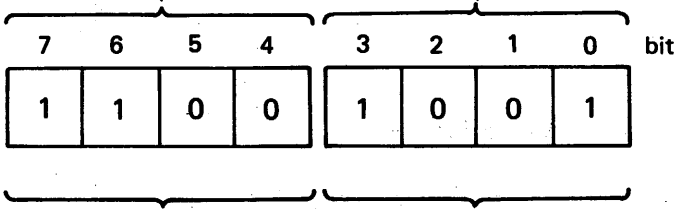
1) To read the data of programmable controller by computer



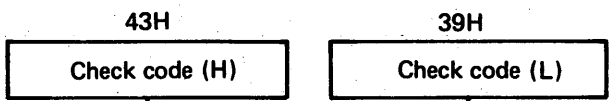
2) Addition of data in terms of binary values

30H
31H
32H
33H
+) 03H
C 9 H

3) Divided into [bit 0 to 3] and [bit 4 to 7]



4) Converted into ASCII code



5) Check codes (L) and (H) are added to address located behind ※marked characters.

6) Example of BASIC

```
10 A$="0123"+CHR$(3)
20 SUM%=0
30 FOR I%=1 TO LEN (A$)
40 SUM%=(SUM%+ASC(MID$(A$, I%, 1))) AND &HFF
50 NEXT I%
60 B$=RIGHT$("0"+HEX$(SUM%), 2)
70 SUM$=RIGHT$(B$, 1)+LEFT$(B$, 1)
80 PRINT SUM$
```

5.4 Character Length

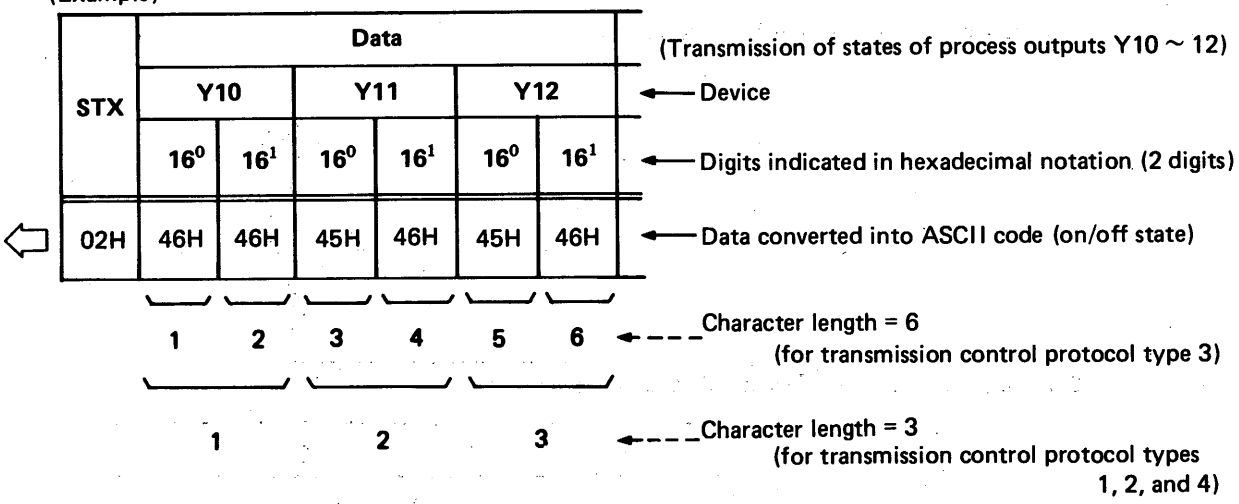
A character length is the number of data in units of bytes, which the KJ71L7 reads or writes on the basis of the request of computer.

- For types 1, 2, and 4 of transmission control protocols, a character length is the number of data bytes indicated in hexadecimal digits.
- For type 3 of transmission control protocol, a character length is the number of data bytes indicated in ASCII code.

To designate the character length, transmit hexadecimal 2 digits after converting them into ASCII code.

(1) Counting of character length

(Example)



(2) Maximum character length

The maximum character length is 256 bytes.

Character length	1	2	3	----------	255	256
Hexadecimal 2 digits	01H	02H	03H	----------	FFH	00H

(3) Number of bytes per data of programmable controller

Data	Bytes/data	Data	Bytes/data
Process input (X)	1	External failure memory (F)	1
Process output (Y)		Master control (K)	
Temporary memory (M)		Temporary value of timer, counter (T, C)	2
Contact, coil of timer, counter (T, C)		Data register (D)	

5.5 Sending Conditions of "NAK"

Table 5.3 shows the factors by which "NAK" is sent from the KJ71L7 to the computer.

(1) To "ENQ" message at the initial (neutral) stage	1) "Write designation" has been received during run of programmable controller when "write during run of programmable controller" is set impossible (switch 4: on) by the designation of transmission specifications (see Table 4.1). (For any protocol type, "NAK" is sent at the timing of 4). See Section 5.1.)
	2) Error has been detected when making "parity check" (switch 2: on) or "sum check" (switch 3: on) by the designation of transmission specifications.
	3) Neither of "read designation" or "write designation" has been selected. (For any protocol type, "NAK" is sent at the timing of 2). See Section 5.1.)
	4) Error has been detected by LSI for serial data transmission. (For example, format error or overrun error)
(2) To "STX" message at the time of "write designation"	1) Error has been detected when making "parity check" (switch 2: on) or "sum check" (switch 3: on) by the designation of transmission specifications.
	2) Data for designated character length has not been sent from the computer.
	3) Other than 0 to F (which is not data) in ASCII code has been sent.
	4) Error has been detected by LSI for serial data transmission. (For example, format error or overrun error)

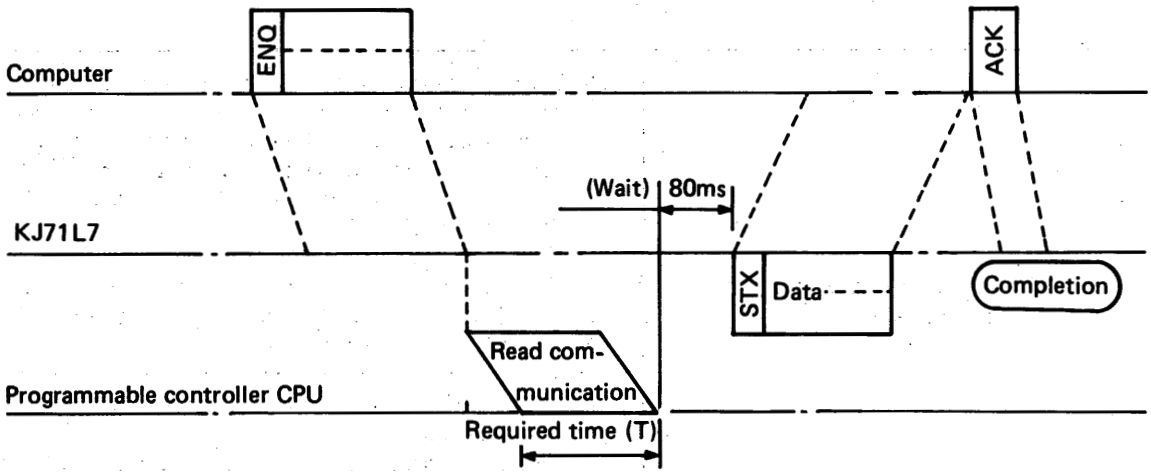
Table 5.3 Factors of Sending "NAK"

Note 1: The initial stage is the state in which the KJ71L7 is ready to receive "ENQ" message from the computer.

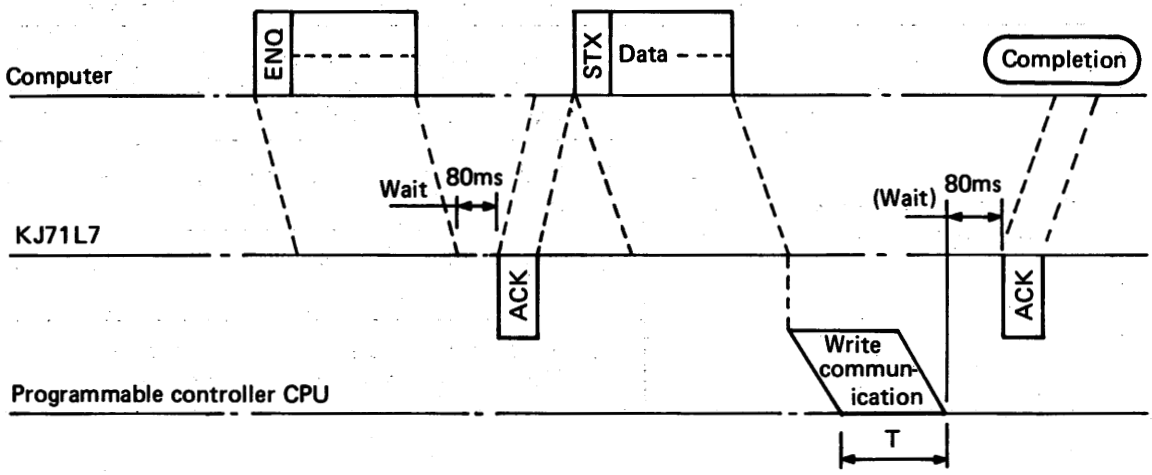
Note 2: After sending "NAK", the KJ71L7 waits for "ENQ" message. There is no restriction on the number of retry times after "NAK" is received. Receive time check is not made.

5.6 Transmission Sequence Time Chart and Communication Time

(1) To read data of programmable controller by computer (during normal run)

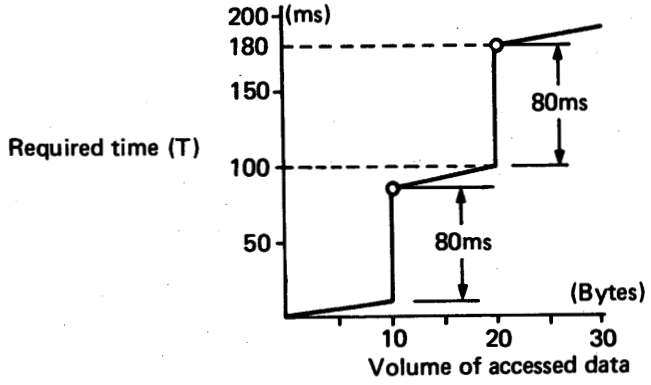


(2) To write data from computer to programmable controller (during normal run)



(3) Required time (T) for read or write communication between KJ71L7 and programmable controller CPU

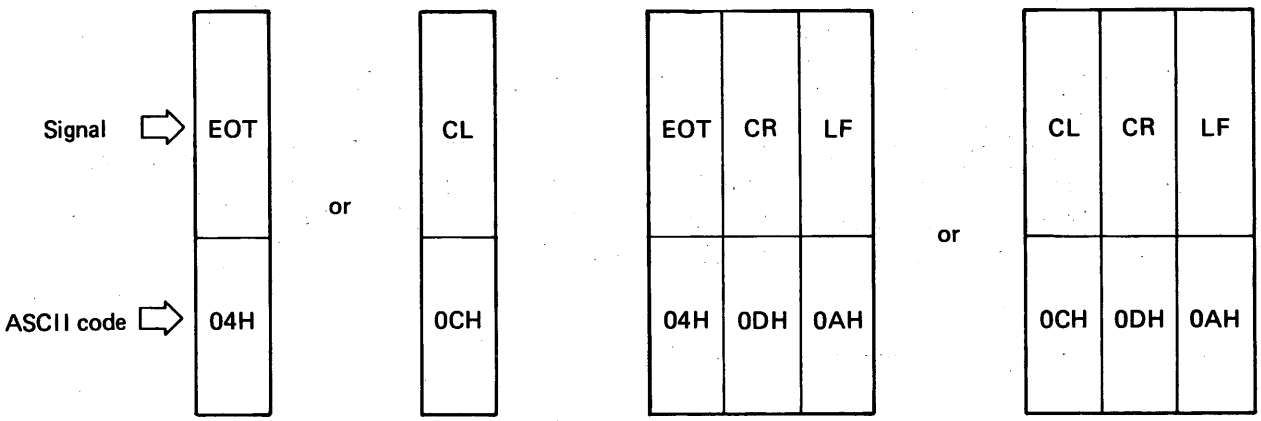
1) Up to 10 bytes are consecutively accessed per read or write.
2) When the number of accessed bytes exceeds 10, 80 ms waiting time is provided per 10 bytes.
3) Approximately 1 ms is required for access to 1 byte.
4) When time check is made by the computer, set fully sufficient value considering the above points.



5.7 Cautions on Link Method

(1) KJ71L7 does not respond to normal procedure

Send one of the following codes and initialize the transmission sequence of KJ71L7 (make the KJ71L7 ready for receiving "ENQ" message from the computer).



Note 1: Initialize the transmission sequence of KJ71L7 after "NAK" is sent and when "NAK" is received. For type 3, however, initialize the transmission sequence after "STX-D-D-ETX" is sent or received and after "STX-Read" designation (Write designation)" is received.

Note 2: Also initialize the transmission sequence when normal sending or receiving has been completed by the transmission control protocol in Section 5.1.

(2) Read processing of 2-byte data

In read or write operation, data processing is carried out per byte in relation to the CPU of programmable controller. Therefore, to read data, which consists of 2 bytes such as the temporary values of timer and counter, the following example may occur. For this reason, it is necessary to take action, for example, to read the data twice, and if these data are equal, use the data.

Example: To read the temporary values of T0

The temporary value is arranged link 7100H (L) / 7101H (H). When a read command is given from the computer with the temporary value at 7100H FF / 7101H 00, first the address 7100 is read as FFH. Then, the address 7101H is read. Assume that before this address is read, a timer instruction has been excuted. In such a case, the temporary value is 7100H 00 / 7101H 01 this time, the address 7101H is read. Therefore, the data 01H is read and the result is FF / 01. Namely, correct data cannot be obtained.

(3) Write during run of programmable controller CPU

If the CPU of programmable controller is running, read or write is possible from the computer as desired. However, use extreme care to the safety of controlled system. When write is not done during run, it is recommended, for the sake of safety, to set switch 4 (see Table 4.1), which is used to designate transmission specifications, to ON position (at this position, write is impossible during run).

(4) Control of "RUN/STOP" switch on programmable controller CPU

During access from the computer, never move the "RUN/STOP" switch on programmable controller CPU from "STOP" to "RUN" position. Be sure to move the switch from "STOP" to "RUN" position after accessing has been completed, i.e. after the LED numbers 0, 1, and 2 in Table 4.2 have turned off and the LED number 3 is lit.

(5) Scan time of programmable controller CPU

When access is provided by the computer after the KJ71L7 computer link unit is loaded, the programmable controller CPU responds to the access.
Even when there is no access, processing time (scan time) lengthens approximately 10% in the K3NCPU, K2NCPU and K2HCPU, and approximately 20% in the K2CPU-S3.
When there is access, processing time lengthens approximately 1 ms per byte. When communication data is 10 bytes or more, processing time is approximately as follows:

Processing time Ts except link is less than 100 ms

K3(N)CPU, K2NCPU, K2HCPU ..... (1.1 x Ts + 10) ms
K2CPU-S3..... .(1.2 x Ts + 10) ms

Processing time Ts except link is 100 ms or more

K3(N)CPU, K2NCPU, K2HCPU ..... (1.1 x Ts + 20) ms

For details of time required for communication between KJ71L7 and programmable controller CPU, see Section 5.6 (3) in page 30.

5.8 Read and Write Operation Examples of Programmable Controller Data by Computer

(1) Example of reading output state of programmable controller by computer

Conditions
- Transmission control protocol: Type 1
- Sum check: Not made
- Programmable controller CPU: K3(N)CPU
- Data to be read: 4 points of Y10 to 13
  (States of 4 points should be as follows:
  Y10 = on, Y11 = off, Y12 = off, Y13 = on)

1) Address of Y10

Y10 = 5000H + 10H = 5010H

- 10H: Begining number of read data Y
- 5000H: Begining address of process output (Y) (See Table 5.1.)

2) Character length

4 points ----- 4-byte data

3) Conversion into ASCII code

Digit	Address		Character Length		On State		Off State	
	Hexadecimal digit	ASCII	Hexadecimal digit	ASCII	Hexadecimal digit	ASCII	Hexadecimal digit	ASCII
16^0	0	30H	4	34H	F	46H	E	45H
16^1	1	31H	0	30H	F	46H	F	46H
16^2	0	30H						
16^3	5	35H						

(3) Transmission data

(Computer → KJ71L7)

(Head)

Character Length		Address				Read Designation	ENQ
16^1	16^0	16^3	16^2	16^1	16^0		
30H	34H	35H	30H	31H	30H	12H	05H

(beginning data)

(Computer ← KJ71L7)

(Head)

STX	Data (On/off State)								ETX
	Y10		Y11		Y12		Y13		
	16^0	16^1	16^0	16^1	16^0	16^1	16^0	16^1	
02H	46H	46H	45H	46H	45H	46H	46H	46H	03H
	F	F	E	F	E	F	F	F	(beginning data)

(2) Example of writing data from computer to data register of programmable controller

Conditions
- Transmission control protocol: Type 1
- Sum check: Not Made
- Programmable controller CPU: K2CPU-S3
- Data register and data to be written: D0 = 100 (64H in hexadecima notation), D1 = 9999 (270FH in hexadecimal notation)

1) Addresses of D0 and D1

D0 = 7200H, 7201H
D1 = 7202H, 7203H (See Table 5.2.)

2) Character length

2 points ---- 4-byte data

3) Conversion into ASCII code

Digit (Indicated in hexadecimal notation)		Address		Character Length		Data			
						D0 (100)		D1 (9999)	
		Hexadecimal Digit	ASCII	Hexadecimal Digit	ASCII	Hexadecimal Digit	ASCII	Hexadecimal Digit	ASCII
1	16^0	0	30H	4	34H	4	34H	F	46H
2	16^1	0	30H	0	30H	6	36H	0	30H
3	16^2	2	32H			0	30H	7	37H
4	16^3	7	37H			0	30H	2	32H

4) Transmission data

(Computer → KJ71L7)

(Head)

Character Length		Address				Write Designation	ENQ
16^1	16^0	16^3	16^2	16^1	16^0		
30H	34H	37H	32H	30H	30H	11H	05H

(beginning data)

(Computer ← KJ71L7) ------ "ACK" has returned from KJ71L7

(Head)

ETX	Data (Contents of data register)								STX
	D1 (9999)				D0 (100)				
	16^3	16^2	16^1	16^0	16^3	16^2	16^1	16^0	
03H	32H	37H	30H	46H	30H	30H	36H	34H	02H

(beginning data)

6. TROUBLE SHOOTING

6. TROUBLE SHOOTING

For the failure of normal communication, various possible causes may be considered. Table 6.1 shows the causes and corrective actions for each trouble. When trouble has occurred, take a proper corrective action according to this table.

Trouble	Cause	Corrective Action
1. LED "0" fails to turn on during sending of KJ71L7.	1) There is wiring error between KJ71L7 and computer.	Perform normal wiring. 1) See Table 4.3 in page 9. 2) See Note 1.
	2) When data is written to programmable controller, there is missing data in specified protocol.	Check and correct computer program. See Section 5.1 in page 11 to 14.
2. LED "1" fails to turn on during receiving of KJ71L7.	1) Receiving line (TB12) is not connected at all or is not connected to the sending terminal of computer.	Securely connect the line. 1) See Table 4.3 in page 9. 2) See Note 1.
	2) Signal is not sent from computer.	Check computer program.
	3) Data set ready (DSR) signal is not on all the time.	Turn on DSR signal of computer all the time.
3. LED "2" fails to turn on during communication with CPU of KJ71L7.	When data is read from programmable controller, there is missing data in specified protocol.	Check and correct computer program. See Section 5.1 in page 11 to 14.
4. KJ71L7 neutral LED "3" fails to turn on.	Hardware failure of KJ71L7	Change KJ71L7 unit.
5. KJ71L7 circuit error LED "10" turns on.	Setting of transmission speed, parity check, sum check, or stop bit is different between KJ71L7 and computer.	Check the setting of transmission specifications. 1) See Table 1 in page 7. 2) See Note 2 and 3.
6. Only "NAK" is sent from KJ71L7.	1) There is unnecessary signal in specified protocol of computer.	Check and correct computer program (protocol). 1) See Section 5.1 in page 11 to 14. 2) See Note 4.
	2) Transmission order of protocol is reverse.	Correct computer program (protocol).
7. Sometimes communication cannot be made and other times not.	1) KJ71L7 is loaded in slot "0" of basic base unit.	Change loading position.
	2) The number of exclusively used inputs/outputs of KJ71L7 is not allotted to be 32 points.	Correct the allocation of input/output numbers.
	3) Data set ready (DSR) singal of KJ71L7 repeats on and off.	Turn on DTR signal of computer all the time.
8. Communication data fails. (Data changes.)	Data has been rewritten by sequence program, thereby resulting in failure.	After checking sending start signal (receiving completion signal) from computer, process the data by sequence program.

Table 6.1 Cause and Corrective Actions of Troubles

Note 1: Checking connection cable between KJ71L7 and computer

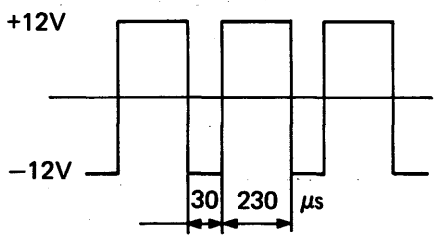
1) Disconnect KJ71L7 from computer and measure terminal voltages (with a circuit tester).

(KJ71L7 side)

Terminal Number	Terinal Name	Signal Name	Measured Value
TB11	FG2	FG	
TB12	TXD2	RD	Approximately 0 V with respect to SG (TB17)
TB13	RXD2	SD	Approximately −12 V with respect to SG (TB17)*1
TB14	RTS2	CS	Approximately 0 V with respect to SG (TB17)
TB15	CTS2	RS	Approximately 7.5 V with respect to SG (TB17)*2
TB16	DSR2	ER	Approximately 7.5 V with respect to SG (TB17)*2
TB17	SG2	SG	(Reference point of measurement)
TB20	DTR2	DR	Approximately 0 V with respect to SG (TB17)

**1: Approximately −12 V means −9 to −12 V.*

**2: The waveform is as shown at right when observed by an oscilloscope. When proper wiring is done and DR signal from computer turns on (3 to 12 V), the voltage is approximately 12 V.*



(Computer side)

Pin Number	Signal Name	Measured Value
1	FG	
2	TXD	Approximately −12 V with respect to SG (pin number 7)*3
3	RXD	Approximately 0 V with respect to SG (pin number 7)
4	RTS	Approximately +12 V with respect to SG (pin number 7)*3
5	CTS	Approximately 0 V with respect to SG (pin number 7)
6	DSR	Approximately 0 V with respect to SG (pin number 7)
7	SG	(Reference point of measurement)
8	CD	Approximately 0 V with respect to SG (pin number 7)
20	DTR	Approximately +12 V with respect to SG (pin number 7)*3

**3: Approximately +12 V means +9 to +12 V and approximately −12 V means −9 to −12 V. Above values may be different on some computers.*

**4: Pin numbers may be different on some computers.*

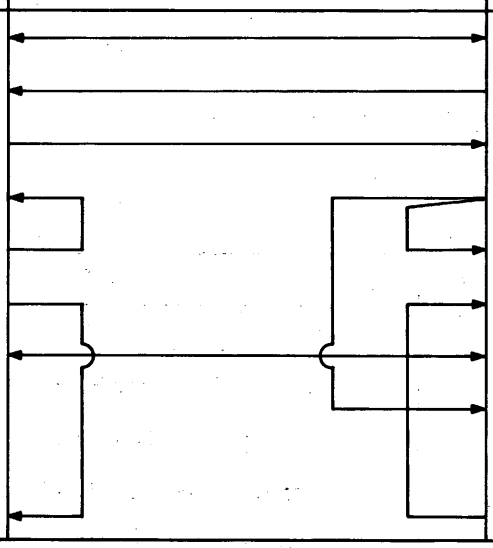
2) Connect KJ71L7 with computer in normal connection method and measure terminal voltages while communication is not made.

Terminal Number	Terminal Name	Signal Name	Measured Value
TB11	FG2	FG	
TB12	TXD2	RD	Approximately –12 V x 3 with respect to SG (TB17)
TB13	RXD2	SD	Approximately –12 V x 3 with respect to SG (TB17)
TB14	RTS2	CS	Approximately +12 V x 3 with respect to SG (TB17)
TB15	CTS2	RS	Approximately +12 V x 3 with respect to SG (TB17)
TB16	DSR2	ER	Approximately +12 V x 3 with respect to SG (TB17)
TB17	SG2	SG	(Reference point of measurement)
TB20	DTR2	DR	Approximately +12 V with respect to SG (TB17)

When the above values are not obtained, SD and RD wires and/or DR and ER wires may be reversely connected. Check pin assignment and signal names.

3) Check if communication can be made in the following connection method of cables between KJ71L7 and computer.

(KJ71L7) (Computer)

Terminal Number	Cable Connection	Pin Number
TB11		1
TB12		2
TB13		3
TB14		4
TB15		5
TB16		6
TB17		7
TB18		8
TB19		
TB20		20

a) If communication can be made by the above connection, wire the cables in normal connection method, observe the waveform of TB20 (DR), and make sure that the waveform is uniform at approximately +12 V. When the waveform is not uniform, recheck the computer program. (Turn on DR of computer all the time.)

b) If communication cannot be made by the above connection, or if communication is made but the voltage waveform of TB20 (DR) is uniform at approximately +12 V, possible cause is the failure of hardware. Therefore, change the KJ71L7 unit.

Note 2: Checking the setting of transmission specifications

1) *Transmission speed is 1200, 2400, 4800, or 9600 BPS. Check if the speed setting of KJ71L7 corresponds to that of computer. When communication cannot be made, make a test at the lowest possible speed in the above speed range.*

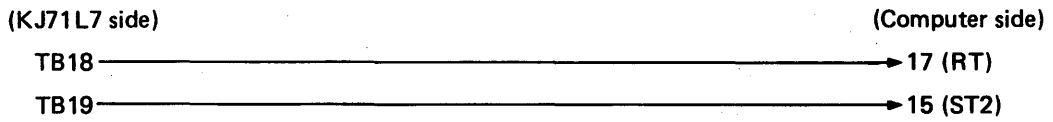
2) *Word length (data bit) is 7 bits irrespective of presence or absence of parity check. Check if word length is set to 7 bits on the computer.*

3) *Check if the setting of presence or absence of parity check is the same on the KJ71L7 and computer. When parity check is "present", even parity is applied.*

4) *Check if the stop bit of KJ71L7 corresponds to that of computer. When communication cannot be made with 2 bits, make a test with 1 bit.*

Note 3: Checking transmission speed

When there is an error between the baud rate clock of KJ71L7 and that of computer, communication may sometimes not be made. In such a case, make a test by lowering the baud rate. When it is impossible to reduce the baud rate, switch the computer to external clock (mode in which a clock is taken from a modem), add the following connection, and proceed to a test.



In this case, it is required for the computer to be capable of taking the baud rate clock of USART (such as i8251 or z80SIO) from pins 17 and 15.

Note 4: Checking the data format of computer program

1) *ODH/OAH, i.e. CR/LF (carriage return/line feed) code which acts as a delimiting code of transmission, is not used for the data format of KJ71L7. Therefore, if this code is provided for the data format, normal communication cannot be made. (This applies only to formats 1 to 3 and does not apply to format 4.)*

   a) *When data is sent in BASIC, be sure to perform programming so that a semicolon (;) is provided at the end in order to prevent the sending of CR/LF.*

      Example: PRINT #1, CHR$(5); CHR$(&H12); "014680" ;

      If this semicolon (;) is not provided, CR/LF is automatically added, and therefore, normal communication cannot be made.

   b) *Note that some computers automatically add CR/LF, as a delimiting code, or a special delimiting code. Select format 4 when making communication by use of CR/LF.*

   c) *The computer may sometimes require CR/LF or a dedicated delimiting code to receive data. When making communication by use of CR/LF, select format 4.*

2) When the specified character length (byte length) does not correspond to the number of received data or the number of written data on the computer in reading or writing the data of programmable controller, check the count of character length in the computer program. The character length corresponds to the number of bytes inside the programmable controller. (See Section 5.4 in page 19.)

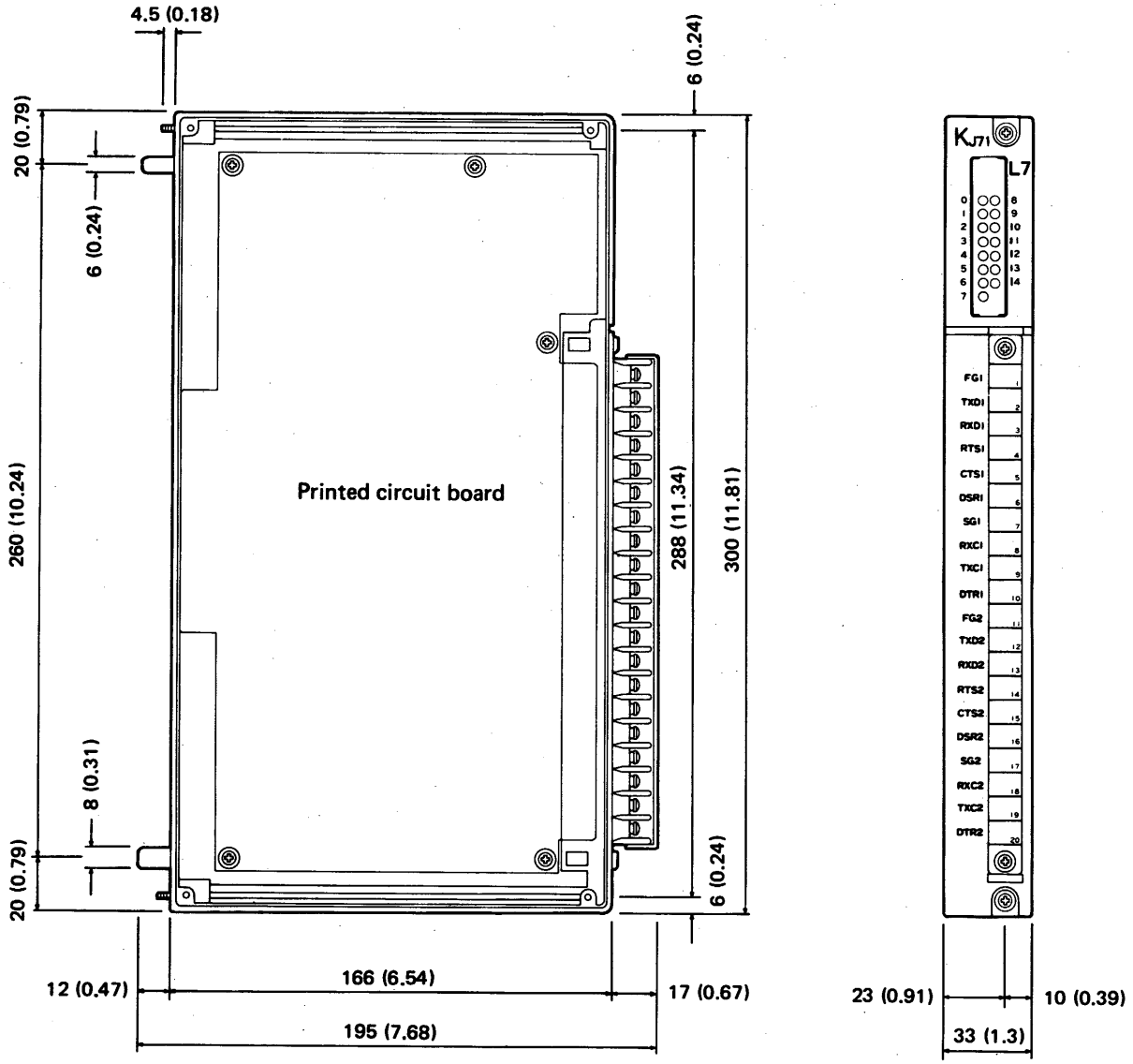
3) When the characters, which have been previously received, remain in the receiving buffer of computer, the order of characters is changed. When "EOT" or "CL" has been sent, it is required to clear the receiving buffer.

Example: In BASIC, enter A$=INPUT$(LOC(1), #1)

7. EXTERNAL DIMENTIONS

7. EXTERNAL DIMENTIONS

Weight: 0.62 kg



mm/(inch)

8. HANDLING INSTRUCTIONS

9. STORAGE

8. HANDLING INSTRUCTIONS

(1) Since the case and terminal block connector of the computer link unit are made of plastic, do not drop or give them strong shock.

(2) During wiring, use care to prevent the entry of foreign matters, such as wire chips, from the top into the unit. If such chips have entered, remove them.

(3) Do not overtighten the unit mounting screws and terminal screws.

(4) Do not remove the printed circuit boards from the case, Removal may cause board failure.

9. STORAGE

When the unit is stored as a single unit or being mounted on the controller, never keep the unit at the locations and environments described below.

(1) Locations where ambient temperature is outside the range of −10°C and 75°C.

(2) Locations where ambient humidity is outside the range of 10% and 90%RH.

(3) Locations where dew condensation takes place due to sudden temperature changes.

(4) Locations exposed to the weather or the direct rays of the sun.

(5) Locations where there are conductive powders such as dust and iron filings, or corrosive gases, oil mist, salt.

IMPORTANT

Since the printed circuit boards within the KJ71L7 are mounted with electronic parts which will be adversely affected by static electricity, handle them as described below when they are directly handled.

(1) Ground human body and work bench.

(2) Do not directly touch the conductive areas of printed circuit board and its electrical parts with a non-grounded material.

MITSUBISHI ELECTRIC CORPORATION
HEAD OFFICE MITSUBISHI DENKI BLDG MARUNOUCHI TOKYO 100 TELEX J24532 CABLE MELCO TOKYO

IB (NA) 66015-A (8502) REC Printed in Japan